

Refine Search

Search Results -

Term	Documents
(10 AND 20).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	0
(L20 AND L10).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	0

Database:

US Pre-Grant Publication Full-Text Database
 US Patents Full-Text Database
 US OCR Full-Text Database
 EPO Abstracts Database
 JPO Abstracts Database
 Derwent World Patents Index
 IBM Technical Disclosure Bulletins

Search:

L24

Refine Search

Recall Text

Clear

Interrupt

Search History

 DATE: Thursday, August 11, 2005 [Printable Copy](#) [Create Case](#)

<u>Set</u> <u>Name</u>	<u>Query</u>	<u>Hit</u> <u>Count</u>	<u>Set</u> <u>Name</u> result set
side by side			
<i>DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR</i>			
<u>L24</u>	L20 and l10	0	<u>L24</u>
<u>L23</u>	L20 and l9	20	<u>L23</u>
<u>L22</u>	L20 and l8	14	<u>L22</u>
<u>L21</u>	L20 and l7	44	<u>L21</u>
<u>L20</u>	L19 and decod\$3	105	<u>L20</u>
<u>L19</u>	l6 and (prefetch\$5 or fetch\$6)	113	<u>L19</u>
<i>DB=PGPB,USPT; PLUR=YES; OP=OR</i>			
<u>L18</u>	l5 and l10	1	<u>L18</u>
<u>L17</u>	l5 and l9	8	<u>L17</u>
<u>L16</u>	l5 and l8	0	<u>L16</u>
<u>L15</u>	l5 and l7	13	<u>L15</u>

Best Available Copy

<u>L14</u>	l6 and l10	1	<u>L14</u>
<u>L13</u>	l6 and l9	29	<u>L13</u>
<u>L12</u>	l6 and l8	14	<u>L12</u>
<u>L11</u>	l6 and l7	48	<u>L11</u>
<u>L10</u>	(711/169,173)[CCLS]	1392	<u>L10</u>
<u>L9</u>	(711/101-173)[CCLS]	21113	<u>L9</u>
<u>L8</u>	(712/207-219)[CCLS]	3276	<u>L8</u>
<u>L7</u>	(712/2-300)[CCLS]	11268	<u>L7</u>
<i>DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR</i>			
<u>L6</u>	(pipelin\$7) near5 (cycle\$1 or clock\$1 or period\$1 or stage\$1) and (instruction\$1 or micronstruction\$1 or macroinstruction\$1 or command\$3) near5 selected near4 (bank\$1 or area\$ or section\$1 or region\$1)	127	<u>L6</u>
<u>L5</u>	(pipelin\$7) near5 (cycle\$1 or clock\$1 or period\$1 or stage\$1) and (read\$6 or retriev\$4 or access\$3) near4 (instruction\$1 or micronstruction\$1 or macroinstruction\$1 or command\$3) near5 selected near4 (bank\$1 or area\$ or section\$1 or region\$1)	46	<u>L5</u>
<u>L4</u>	(pipelin\$7) near5 (cycle\$1 or clock\$1 or period\$1 or stage\$1) and (read\$6 or retriev\$4 or access\$3) near4 (instruction\$1 or micronstruction\$1 or macroinstruction\$1 or command\$3) near5 selected near4 (bank\$1)	43	<u>L4</u>
<u>L3</u>	(pipelin\$7) near5 (cycle\$1 or clock\$1 or period\$1 or stage\$1) near25 (read\$6 or retriev\$4 or access\$3) near4 (instruction\$1 or micronstruction\$1 or macroinstruction\$1 or command\$3) near5 selected near4 (bank\$1)	1	<u>L3</u>
<u>L2</u>	(read\$6 or retriev\$4 or access\$3) near4 (instruction\$1 or micronstruction\$1 or macroinstruction\$1 or command\$3) near7 (without or "NOT") near5 (unselected or selected) near4 (bank\$1)	3	<u>L2</u>
<u>L1</u>	(read\$6 or retriev\$4 or access\$3) near4 (instruction\$1 or micronstruction\$1 or macroinstruction\$1 or command\$3) near7 (only) near5 selected near4 (bank\$1)	7	<u>L1</u>

END OF SEARCH HISTORY


[Home](#) | [Login](#) | [Logout](#) | [Access Information](#) | [Alt](#)

Welcome United States Patent and Trademark Office

Search Results

BROWSE

SEARCH

IEEE XPLORE GUIDE

Results for "((bank* <near/5> memor* <and> pipelin*)<in>metadata)"

e-mail

Your search matched 28 of 1222090 documents.

A maximum of 100 results are displayed, 25 to a page, sorted by Relevance in Descending order.

» Search Options

[View Session History](#)
[New Search](#)

Modify Search


☐ Check to search only within this results set

Display Format:



Citation



Citation & Abstract

» Key

IEEE JNL	IEEE Journal or Magazine
IEEE JNL	IEEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEEE CNF	IEEE Conference Proceeding
IEEE STD	IEEE Standard

Select Article Information



1. A hardware accelerator for maze routing

Won, Y.; Sahni, S.; El-Ziq, Y.;
Computers, IEEE Transactions on
Volume 39, Issue 1, Jan. 1990 Page(s):141 - 145
Digital Object Identifier 10.1109/12.46291

[AbstractPlus](#) | Full Text: [PDF](#)(520 KB) IEEE JNL


2. Block, multistride vector, and FFT accesses in parallel memory systems

Harper, D.T., III;
Parallel and Distributed Systems, IEEE Transactions on
Volume 2, Issue 1, Jan. 1991 Page(s):43 - 51
Digital Object Identifier 10.1109/71.80188

[AbstractPlus](#) | Full Text: [PDF](#)(836 KB) IEEE JNL


3. Scalar memory references in pipelined multiprocessors: a performance study

Ganesan, R.; Weiss, S.;
Software Engineering, IEEE Transactions on
Volume 18, Issue 1, Jan. 1992 Page(s):78 - 86
Digital Object Identifier 10.1109/32.120318

[AbstractPlus](#) | Full Text: [PDF](#)(712 KB) IEEE JNL


4. Models of access delays in multiprocessor memories

Bucher, I.Y.; Calahan, D.A.;
Parallel and Distributed Systems, IEEE Transactions on
Volume 3, Issue 3, May 1992 Page(s):270 - 280
Digital Object Identifier 10.1109/71.139201

[AbstractPlus](#) | Full Text: [PDF](#)(912 KB) IEEE JNL


5. The GLUEchip: a custom VLSI chip for detector readout and associative memories circuits

Amendolia, S.R.; Galeotti, S.; Morsani, F.; Passuello, D.; Ristori, L.; Sciacca, G.; Turini, N.;
Nuclear Science, IEEE Transactions on
Volume 40, Issue 4, Part 1-2, Aug 1993 Page(s):733 - 735
Digital Object Identifier 10.1109/23.256651

[AbstractPlus](#) | Full Text: [PDF](#)(168 KB) IEEE JNL


6. Multiskewing-a novel technique for optimal parallel memory access

Deb, A.;

Parallel and Distributed Systems, IEEE Transactions on
Volume 7, Issue 6, June 1996 Page(s):595 - 604
Digital Object Identifier 10.1109/71.506698

[AbstractPlus](#) | Full Text: [PDF](#)(852 KB) [IEEE JNL](#).



7. An efficient pipelined parallel architecture for blocking effect removal in HDTV

Jae-Wook Lee; Myung-Hoon Yang; Sungho Kang; Yoonsik Choe;
Consumer Electronics, IEEE Transactions on
Volume 43, Issue 2, May 1997 Page(s):149 - 156
Digital Object Identifier 10.1109/30.585533

[AbstractPlus](#) | Full Text: [PDF](#)(736 KB) [IEEE JNL](#).



8. Efficient algorithm and architecture for post-processor in HDTV

Jae-Wook Lee; Jeong-Woo Park; Myung-Hoon Yang; Sungho Kang; Yoonsik Choe;
Consumer Electronics, IEEE Transactions on
Volume 44, Issue 1, Feb. 1998 Page(s):16 - 26
Digital Object Identifier 10.1109/30.663726

[AbstractPlus](#) | Full Text: [PDF](#)(1164 KB) [IEEE JNL](#).



9. A pipeline of associative memory boards for track finding

Annovi, A.; Bagliesi, M.G.; Bardi, A.; Carosi, R.; Dell'Orso, M.; Gannetti, P.; Iannaccone, G.; Moran Varano, G.;
Nuclear Science, IEEE Transactions on
Volume 48, Issue 3, Part 1, June 2001 Page(s):595 - 600
Digital Object Identifier 10.1109/23.940125

[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(160 KB) [IEEE JNL](#).



10. Efficient algorithm and architecture for scan conversion in HDTV

Yang, M.-H.; Lee, J.-W.; Kang, S.;
Computers and Digital Techniques, IEE Proceedings-
Volume 145, Issue 4, July 1998 Page(s):287 - 291

[AbstractPlus](#) | Full Text: [PDF](#)(880 KB) [IEEE JNL](#).



11. Logic-enhanced memory for 3D graphics tile-based rasterizers

Crisu, D.; Cotofana, S.; Vassiliadis, S.; Liuha, P.;
Circuits and Systems, 2004. MWSCAS '04. The 2004 47th Midwest Symposium on
Volume 2, 25-28 July 2004 Page(s):II-237 - II-240 vol.2
Digital Object Identifier 10.1109/MWSCAS.2004.1354136

[AbstractPlus](#) | Full Text: [PDF](#)(535 KB) [IEEE CNF](#)



12. HDL synthesis and simulation of eight bit DSP based micro-controller for image processing

Rangarajan, P.; Kutraleeshwaran, V.; Vaasanthy, K.; Perinbam, R.P.;
Circuits and Systems, 2002. MWSCAS-2002. The 2002 45th Midwest Symposium on
Volume 3, 4-7 Aug. 2002 Page(s):III - 609-12 vol.3
Digital Object Identifier 10.1109/MWSCAS.2002.1187113

[AbstractPlus](#) | Full Text: [PDF](#)(282 KB) [IEEE CNF](#)



13. Design of a parallel vector access unit for SDRAM memory systems

Mathew, B.K.; McKee, S.A.; Carter, J.B.; Davis, A.;
High-Performance Computer Architecture, 2000. HPCA-6. Proceedings. Sixth International Sympo:
8-12 Jan. 2000 Page(s):39 - 48
Digital Object Identifier 10.1109/HPCA.2000.824337

[AbstractPlus](#) | Full Text: [PDF](#)(116 KB) [IEEE CNF](#)



14. A pipeline of associative memory boards for track finding

Annovi, A.; Bagliesi, M.G.; Bardi, A.; Carosi, R.; Dell'Orso, M.; Giannetti, P.; Iannaccone, G.; Morsa Varotto, G.;
Nuclear Science Symposium Conference Record, 2000 IEEE

Volume 2, 15-20 Oct. 2000 Page(s):12/227 - 12/231 vol.2

Digital Object Identifier 10.1109/NSSMIC.2000.949977

[AbstractPlus](#) | Full Text: [PDF](#)(496 KB) IEEE CNF



15. A C to HDL compiler for pipeline processing on FPGAs

Maruyama, T.; Hoshino, T.;

Field-Programmable Custom Computing Machines, 2000 IEEE Symposium on
17-19 April 2000 Page(s):101 - 110

Digital Object Identifier 10.1109/FPGA.2000.903397

[AbstractPlus](#) | Full Text: [PDF](#)(696 KB) IEEE CNF



16. Implementation of 13 kbps QCELP vocoder ASIC

Kyung-Jin Byun; Minsoo Hahn; Kyung-Su Kim;

ASICs, 1999. AP-ASIC '99. The First IEEE Asia Pacific Conference on
23-25 Aug. 1999 Page(s):258 - 261

Digital Object Identifier 10.1109/APASIC.1999.824078

[AbstractPlus](#) | Full Text: [PDF](#)(340 KB) IEEE CNF



17. Low-power full-search motion estimator architecture suitable for random-block match

Kyung-Saeng Kim; Dong-Jae Lee; Hoi-Jun Yoo; Kwyro Lee;

ASICs, 1999. AP-ASIC '99. The First IEEE Asia Pacific Conference on
23-25 Aug. 1999 Page(s):210 - 212

Digital Object Identifier 10.1109/APASIC.1999.824065

[AbstractPlus](#) | Full Text: [PDF](#)(268 KB) IEEE CNF



18. Mapping the MD5 hash algorithm onto the NAPA architecture

Arnold, J.M.;

FPGAs for Custom Computing Machines, 1998. Proceedings. IEEE Symposium on
15-17 April 1998 Page(s):267 - 268

Digital Object Identifier 10.1109/FPGA.1998.707910

[AbstractPlus](#) | Full Text: [PDF](#)(92 KB) IEEE CNF



19. Architecture and performance of the Hitachi SR2201 massively parallel processor system

Fujii, H.; Yasuda, Y.; Akashi, H.; Inagami, Y.; Koga, M.; Ishihara, O.; Kashiwayama, M.; Wada, H.; Su;

Parallel Processing Symposium, 1997. Proceedings., 11th International
1-5 April 1997 Page(s):233 - 241

Digital Object Identifier 10.1109/PPS.1997.580901

[AbstractPlus](#) | Full Text: [PDF](#)(836 KB) IEEE CNF



20. An object-oriented data cache architecture for programmable parallel digital signal processing

Kneip, J.;

Algorithms and Architectures for Parallel Processing, 1997. ICAPP 97. 1997 3rd International Conference on
10-12 Dec. 1997 Page(s):105 - 112

Digital Object Identifier 10.1109/ICAPP.1997.651483

[AbstractPlus](#) | Full Text: [PDF](#)(532 KB) IEEE CNF



21. Programmable architecture for matrix and signal processing

Hamilton, B.;

IEEE Region 5 Conference, 1988: 'Spanning the Peaks of Electrotechnology'
21-23 March 1988 Page(s):116 - 120

Digital Object Identifier 10.1109/REG5.1988.15912

[AbstractPlus](#) | Full Text: [PDF](#)(384 KB) IEEE CNF



22. Parallel computation of neural networks in a processor pipeline with partially shared memory

Okawa, Y.; Suyama, H.;

Tools for Artificial Intelligence, 1990., Proceedings of the 2nd International IEEE Conference on
6-9 Nov. 1990 Page(s):276 - 282

Digital Object Identifier 10.1109/TAI.1990.130347

[AbstractPlus](#) | Full Text: [PDF\(420 KB\)](#) IEEE CNF



23. Architecture synthesis of high-performance application-specific processors

Breternitz, M., Jr.; Shen, J.P.;

Design Automation Conference, 1990. Proceedings. 27th ACM/IEEE

24-28 June 1990 Page(s):542 - 548

Digital Object Identifier 10.1109/DAC.1990.114915

[AbstractPlus](#) | Full Text: [PDF\(668 KB\)](#) IEEE CNF



24. GFLOPS: a general flexible linearly organized parallel structure for images

Houzet, D.; Basille, J.-L.; Latil, J.-Y.;

Application Specific Array Processors, 1991. Proceedings of the International Conference on
2-4 Sept. 1991 Page(s):431 - 444

Digital Object Identifier 10.1109/ASAP.1991.238904

[AbstractPlus](#) | Full Text: [PDF\(612 KB\)](#) IEEE CNF



25. Fault tolerant multi-processor communication systems using bank memory switching

Tanaka, N.; Kurokawa, T.; Koga, Y.;

Fault Tolerant Systems, 1991. Proceedings., Pacific Rim International Symposium on
26-27 Sept. 1991 Page(s):188 - 193

Digital Object Identifier 10.1109/RFTS.1991.212958

[AbstractPlus](#) | Full Text: [PDF\(348 KB\)](#) IEEE CNF



Indexed by
 Inspec®

[Help](#) [Contact Us](#) [Privacy](#)

© Copyright 2005 IE


[Home](#) | [Login](#) | [Logout](#) | [Access Information](#) | [Alt](#)

Welcome United States Patent and Trademark Office

Search Results

BROWSE

SEARCH

IEEE XPLORE GUIDE

Results for "((bank* <near/5> memor* <and> pipelin*)<in>metadata)"

e-mail

Your search matched 28 of 1222090 documents.

A maximum of 28 results are displayed, 25 to a page, sorted by Relevance in Descending order.

» Search Options

[View Session History](#)[New Search](#)

Modify Search

((bank* <near/5> memor* <and> pipelin*)<in>metadata)

☐ Check to search only within this results set

» Key

Display Format:



Citation



Citation & Abstract

IEEE JNL IEEE Journal or Magazine

IEEE JNL IEEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEEE CNF IEEE Conference Proceeding

IEEE STD IEEE Standard

Select Article Information

**26. Parallel computation of neural networks in a processor pipeline with partially shared memor**

Okawa, Y.; Suyama, T.;
Neural Networks, 1993., IEEE International Conference on
28 March-1 April 1993 Page(s):1638 - 1643 vol.3
Digital Object Identifier 10.1109/ICNN.1993.298802

[AbstractPlus](#) | Full Text: [PDE\(404 KB\)](#) IEEE CNF**27. Enhancement of the weight cell utilization for CMAC neural networks: architecture design and implementation**

Jar-Shone Ker; Rong-Chang Wen; Yau-Hwang Kuo; Bin-Da Liu;
Microelectronics for Neural Networks and Fuzzy Systems, 1994., Proceedings of the Fourth Interna
26-28 Sept. 1994 Page(s):244 - 251
Digital Object Identifier 10.1109/ICMNN.1994.593716

[AbstractPlus](#) | Full Text: [PDE\(640 KB\)](#) IEEE CNF**28. An interprocessor memory access arbitrating scheme for the S-3800 vector supercomputer**

Sakakibara, T.; Kitai, K.; Isobe, T.; Yazawa, S.; Tanaka, T.; Tamaki, Y.; Inagami, Y.;
Parallel Architectures, Algorithms and Networks, 1994. (ISPAN) International Symposium on
14-16 Dec. 1994 Page(s):262 - 269
Digital Object Identifier 10.1109/ISPAN.1994.367140

[AbstractPlus](#) | Full Text: [PDE\(456 KB\)](#) IEEE CNF[Help](#) [Contact Us](#) [Privacy](#)

© Copyright 2005 IEEE

 indexed by

**This Page is Inserted by IFW Indexing and Scanning
Operations and is not part of the Official Record**

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- ☒ **BLACK BORDERS**
- ☐ **IMAGE CUT OFF AT TOP, BOTTOM OR SIDES**
- ☐ **FADED TEXT OR DRAWING**
- ☐ **BLURRED OR ILLEGIBLE TEXT OR DRAWING**
- ☐ **SKEWED/SLANTED IMAGES**
- ☐ **COLOR OR BLACK AND WHITE PHOTOGRAPHS**
- ☐ **GRAY SCALE DOCUMENTS**
- ☐ **LINES OR MARKS ON ORIGINAL DOCUMENT**
- ☐ **REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY**
- ☐ **OTHER:** _____

IMAGES ARE BEST AVAILABLE COPY.

As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.